WHAT IS CLAIMED IS:

1. A phase adjustment circuit for receiving a first pair of clock signals and outputting a second pair of clock signals with phases satisfying a predetermined condition, comprising:

a clock proliferator for receiving a first clock signal and generating a plurality of clock signals therefrom;

a clock selector for receiving said plurality of clock signals from the clock proliferator, selecting one of the received plurality of clock signals in accordance with a selection signal, and outputting the selected clock signal; and

a phase difference detector for receiving the selected clock signal and a second clock signal, determining whether the phase of the second clock signal and the phase of the selected clock signal satisfy the predetermined condition, and outputting a detection signal indicating whether the predetermined condition is satisfied;

the first clock signal and the second clock signal constituting the first pair of clock signals;

the second clock signal and the selected clock signal constituting the second pair of clock signals.

2. The phase adjustment circuit of claim 1, wherein the clock proliferator generates the plurality of clock signals by delaying the first clock signal by different amounts.

3. The phase adjustment circuit of claim 2, wherein the clock proliferator comprises a cascaded plurality of delay elements.

4. The phase adjustment circuit of claim 1, further comprising:

an external input terminal for input of the selection signal; and

an external output terminal for output of the detection signal.

5. The phase adjustment circuit of claim 1, further comprising:

an externally writable register for storing the selection signal and supplying the selection signal to the clock selector; and

an external output terminal for output of the detection signal.

6. The phase adjustment circuit of claim 1, wherein the phase difference detector comprises:

a first flip-flop for latching and outputting the state of the second clock signal at rising edges of the selected clock signal;

a second flip-flop for latching and outputting the state of the second clock signal at falling edges of the selected clock signal; and

a logic circuit for performing a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

7. The phase adjustment circuit of claim 6, wherein the first clock signal has a lower frequency than the second clock signal.

8. The phase adjustment circuit of claim 1, wherein the phase difference detector comprises:

a first flip-flop for latching and outputting the state of the selected clock signal at rising edges of the second clock signal;

a second flip-flop for latching and outputting the state of the selected clock signal at falling edges of the second clock signal; and

a logic circuit for performing a logic operation on outputs of the first flip-flop and the second flip-flop, thereby generating the detection signal.

9. The phase adjustment circuit of claim 8, wherein the first clock signal has a higher frequency than the second clock signal.

10. The phase adjustment circuit of claim 1, further comprising a selection signal generator for receiving the detection signal and generating the selection signal.

11. The phase adjustment circuit of claim 10, wherein the selection signal generator cyclically increases or decreases the selection signal within a certain range of values while the detection signal indicates that the predetermined condition is not satisfied, and holds the selection signal constant while the detection signal indicates that the predetermined condition is satisfied.

12. The phase adjustment circuit of claim 10, wherein the selection signal generator comprises:

a register for storing the value of the selection signal;

an adder for adding a fixed value to the value stored in the register to generate a sum value; and

a selector for receiving the value stored in the register and the sum value, selecting the value stored in the register when the detection signal indicates that the predetermined condition is satisfied, selecting the sum value when the detection signal indicates that the

predetermined condition is not satisfied, writing the selected value in the register, and supplying the selected value to the clock selector as the selection signal.